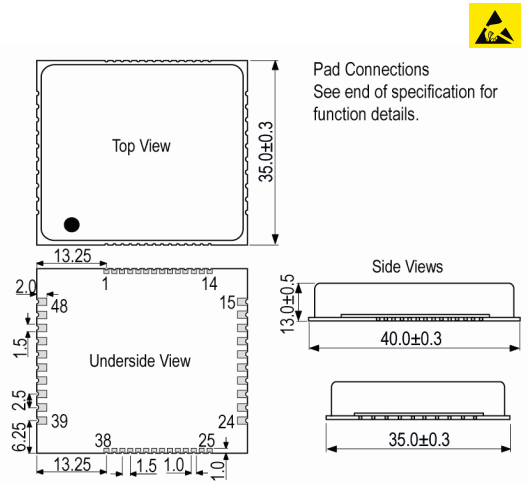
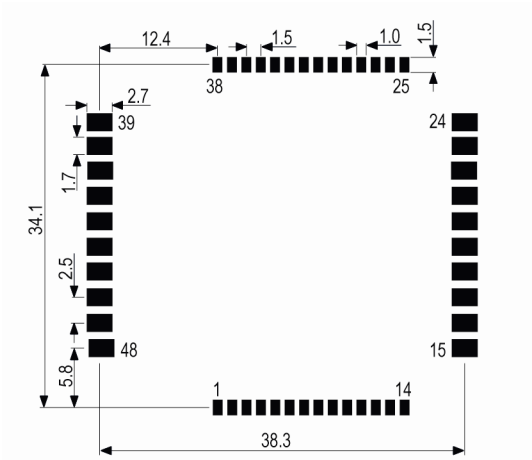
ISSUE 1; June 2019

Outline (mm)



Solder Pad Layout



Description

- The IQCM-310 is a high-performance clock module designed to provide precise frequency, phase and time-of-day synchronization information for telecom and other applications. It combines the IEEE 1588-2008 (1588V2) with advanced PTP IC and adaptive timing algorithms which uses 1PPS retrieving from GNSS as a primary time reference. The module supports PTP Grandmaster, PTP Slave and BC.
- Key features
  Timebase derived from: PTP slave, BITS/SSU input, GNSS timing satellite signal.
  PTP Grandmaster: PTP Grandmaster function supports multiple PTP slaves using multicast or unicast messaging. Timebase may be PTP or ARB.
  PTP Slave: Acting as a PTP Ordinary Clock in Slave mode, IQCM-310 can lock to BCs, or it can use sophisticated packet delay filters and adaptation algorithms to lock to a remote PTP Grandmaster over a multi-hop legacy network which has no PTP support.
- Time-aligned output pair (pads 17, 18): 1 PPS and 125 MHz divided by n (n = 4 to 125000). Maximum of 125MHz (divide by 4); minimum of 100 Hz (divide by 1249999).
  Frequency-aligned outputs: 1 Hz and programmable frequency 1 kHz to 62.5MHz.
  Supports ITU profiles: G.8265.1,G.8275.1, and G.8275.2.
  Clocks: 3 clock inputs and 4 clock outputs.
  Ports: 2xSGMII and 2xUART(1xTOD).
  Management Interface: UART
- Note1: The IQCM-310 should be left powered and running for 7 days minimum before operation to allow for the OCXO's internal drift to stabilise.
  Note2: The adaptive module algorithm can be built after two days operation with good GPS signal, however this data will be lost at power down.

Frequency Parameters

- Frequency 10.0MHz
- Recovery Precision 24 Hours (□T=±5□□Test after Power on 30 min): ±50ns max
- Holdover Capability Time 8 hours (□T=±5□□Test after Power on and lock 2 days): ±1.5μs (Supports external clock with advanced holdover compensation algorithm)

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Electrical Parameters

- Supply Voltage 3.3V ±5%
- Current Consumption local oscillator:
  2000mA max during warm-up
  1000 mA max during steady state operation @ 25□

  Current Consumption external reference:
  1000mA max during warm-up
  1000mA max during steady state operation @ 25□

  AC Ripple (10kHz to 1MHz): 50mV pk-pk max
- Reset (pad 46): the clock module must be active low for a minimum of 2µs. If Reset is forced low, all internal states are reset to default values.
- Locked status (pad 42): Indicates that the device has achieved lock to the selected reference (active high). The degree of lock indicated is software defined. The LOCKED pad is used in PTP only.
- Clock Select (pad 20):
  Logic 1: the system clock uses the local oscillator.
  Logic 0: the system clock uses the external reference.
- Input Clocks (pads 43, 44):
  Single-ended input. Acceptable frequencies into the PTP module from 1PPS/1 Hz to 161MHz (input reference for PTP Master).
  The input frequencies must obey the following rule: Input Freq = k * 2^n, where 0 <= n <= 5 and 1 <= k <= 2^32 (upper limit of 170 MHz).
- Input Clocks (pads 6, 7): Differential input. TDM module only. Programmable input frequencies to a maximum of 155.52MHz.
  Default 19.44 MHz. Default signal type LVDS.
- Output Clock (pads 32, 33): LVDS differential output. Default frequency 77.76MHz
- System Clock (pad 21): External clock (support frequency 10MHz only),
  back up for the local oscillator.
- Time-aligned output pair (pads 17, 18): 125 MHz divided by n (n = 4 to 125000). Maximum of 25MHz (divide by 4); minimum of 100 Hz (divide by 1249999). Frequency-aligned outputs: programmable frequency 1 kHz to 62.5MHz.

Operating Temperature Ranges

- -20 to 75°C

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Output Details

- DC characteristics of the TTL ports:
  TTL input port:
  VIN High: 2.0V min
  VIN Low: 0.8V max
  Input current:10µA max

  TTL input port with internal pull-up:
  VIN High: 2.0V min
  VIN Low: 0.8V max
  Pull-up resistor: 20kΩ min, 200kΩ max
  Input current: 100µA max
- TTL input port with internal pull-down:
  VIN High: 2.0V min
  VIN Low: 0.8V max
  Pull-down resistor: 20kΩ min, 200kΩ max
  Input current: 100µA max

  TTL output port (OPCLK, 1PPSOUT):
  VOUT Low (IOL = 8 mA): 0V min, 0.4V max
  VOUT High (IOH= 8 mA): 2.4V min
  Drive current: -8mA min, 8mA max

  TTL output port (other pins):
  VOUT Low (IOL = 4 mA): 0V min, 0.4V max
  VOUT High (IOH= 4 mA): 2.4V min
  Drive current: 4mA max
- DC characteristics of the LVDS ports
  LVDS input voltage range (Differential input voltage=100mV): 0V min, 2.4V max
  LVDS differential input threshold: -100mV min, 100mV max
  LVDS input differential voltage: 0.1V min, 1.4V max
  LVDS input termination resistance: 95Ω min, 100Ω typ, 105Ω max
- LVDS output high voltage: 1.585V max
  LVDS output low voltage: 0.885V min
  LVDS differential output voltage: 250mV min, 450mV max
  LVDS change in magnitude of differential output voltage for complementary states: 25mV max
  LVDS output offset voltage (@ 25□): 1.125V min, 1.375V max
- SGMII interface (pads 9, 10, 12, 13, 26, 27, 29, 30):
  The IQCM-310 has two serial SGMII interfaces running with a 100Mbps data rate and a 1.25Gbps line rate. The interfaces are IEEE 802.3 compliant for communication via a suitable packet PHY.
- SGMII output data AC characteristics:
  Serial data rate:1.25 Gbits/sec typ
  Vod fall time (80% to 20%): 100ps min, 200ps max
  Vod rise time (20% to 80%): 100ps min, 200ps max
  Skew between two members of a differential pair: ±20ps max
- SGMII input data AC characteristics:
  Serial input data rate tolerance: -300ppm min, +300ppm max
- SGMII input data DC characteristics:
  Input voltage range: 675mV min, 1725mV max
  Input differential threshold: 50mV min, 400mV max
  Input differential voltage (VOD): 150mV min, 400mV max
  Differential input impedance: 80Ω min, 120Ω max
- Time of day: A TOD port is used in PTP Timing modes only. In PTP GM mode, the port is an input comprising UART RX and a 1PPS signal. In PTP Slave mode, the port is an output comprising UART TX and a PPnS signal, which gives a pulse every n seconds (tW configurable for a minimum of 100ns to a maximum of 400ms). The UART has a fixed baud rate (9600) using 1 stop bit and no parity.
- A TOD message format can be a GPRMC message or one of a group of other GPS messages or proprietary messages to suit specific causes. A GPRMC message has the format:
  $GPRMC,122356,A,0000.0000,N,00000.0000,W,0.0.0.0,120508,,,A*F6 in which the commas are separators. The message is 62 characters in length (i.e. 62 bytes). No parity bit is used, but each byte has a stop bit.

- Architecture of GPRMC message:
  $GPRMC: message header
  122356: UTC value
  A: Status (A=active, V=void)
  0000.0000,N: Latitude, north (fixed to zero)
  0000.0000,W: Longitude, west (fixed to zero)
  0.0: Speed ove grund (fixed to zero)
  0.0: Track angle (fixed to zero)
  120508: Date (ddmmyy)
  A: A=autonomnous, D=differential, E=estimated, S=simulation, N=not valid
  *F6: Checksum

Output Control

- UART (pads 23, 24, 39, 40): The UART is used for configuration management, which has a fixed baud rate (9600) using 1 stop bit and no parity. It is a LVTTL-compatible port and needs an external translator to work with other signal types such as RS-232C or RS-485

Output Levels

- SGMII output data DC characteristics:
  Output voltage high state (Voh): 1525mV max
  Output voltage low state (Vol): 875mV min
  Output differential voltage (VOD): 150mV min, 400mV max

Noise Parameters

- Jitter tolerance of the 1PPS input:
  The IQCM-310 will reject a 1PPS signal if the jitter is greater than 4µs peak-to-peak. However it is strongly recommended that jitter on this signal is avoided as much as possible because the distribution of jitter on this signal is not known and so cannot be correctly attenuated by filtering. Any filtering applied to this signal will introduce a phase offset error.
- This treatment differs from that of more traditional reference sources because the phase of a 1PPS signal, relative to a recognized source of time such as UTC, is the parameter of most significance. For other references, the rate (frequency) is the more significant parameter.

Environmental Parameters

- Operating Temperature Range: -20 to 75°C
- Storage Conditions:
  Temperature: -55 to 105°C
  Humidity: 30 to 80%
- Vibration: IEC 68-2-06 Test Fc, 10G, 0.75mm acceleration, 10Hz to 500Hz, 3 times in three mutually perpendicular axies
- Shock: IEC68-2-27 Test Ea, severity 50A: 50g, 11ms half sinewave, 3 times in three mutually perpendicular axes.

Manufacturing Details

- ESD Level:
  Human Body Model (HBM): ANSI/ESDA/JEDEC JS-001-2010; HBM class 2, 2kV to 4kV
  Machine Model (MM): ANSI/ESDA/JEDEC JS-001-2010; MM class B, 200V to 400V

Compliance

- RoHS Status (2015/863/EU) Compliant
- REACh Status Compliant
- MSL Rating (JDEC-STD-033): Not Applicable

Packaging Details

- Pack Style: Bulk Bulk pack
  Pack Size: 1

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Pin Configuration

Pad Group	Pad Name	Pad Number	Pad Type	Description	
Power Supply	+Vs	47, 48	Power	3.3V Power Supply	
Ground	GND	5, 8, 11, 14, 22, 25, 28, 31, 34, 41, 45	Power	Ground	
Control & Alarm Pads	CLK_SEL	20	Input	System clock select	
Control & Alarm Pads	LOCKED	42	Output	State output	
Control & Alarm Pads	RST	46	Input	Reset the clock module	
SGMII	SGMII Tx P1	9	Output	PTP port, SGMII	
SGMII	SGMII Tx N1	10	Output	PTP port, SGMII	
SGMII	SGMII Rx P1	12	Input	PTP port, SGMII	
SGMII	SGMII Rx N1	13	Input	PTP port, SGMII	
SGMII	SGMII Tx P0	26	Output	PTP port, SGMII	
SGMII	SGMII Tx N0	27	Output	PTP port, SGMII	
SGMII	SGMII Rx P0	29	Input	PTP port, SGMII	
SGMII	SGMII Rx N0	30	Input	PTP port, SGMII	
UART 9600-N-8-1	TOD0_Rx	23	Input	Time of day output/input	
UART 9600-N-8-1	TOD0_Tx	24	Output	Time of day output/input	
UART 9600-N-8-1	UART0_Rx	39	Input	Configuration management	
UART 9600-N-8-1	UART0_Tx	40	Output	Configuration management	
Input Clocks	IPCLK0	43	Input	Input Clocks 1PPS	
Input Clocks	IPCLK1	44	Input	Input Clocks 1PPS	
Input Clocks	IPCLK_P	6	Input	Input Clocks LVDS	
Input Clocks	IPCLK_N	7	Input	Input Clocks LVDS	
Output Clocks	1PPS_OUT0	15	Output	PPS Reference Output	
Output Clocks	1PPS_OUT1	16	Output	PPS Reference Output	
Output Clocks	OPCLK0	17	Output	Time Aligned Pair	
Output Clocks	OPCLK1	18	Output	Time Aligned Pair	
Output Clocks	OPCLK_P	32	Output	LVDS Output	

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Output Clocks	OPCLK_N	33	Output	LVDS Output	
System Clock	EXT_CLK	21	Input	External Clock 10MHz	
Reserve	NC	1, 2, 3, 4, 19, 35, 36, 37, 38	No connection	Reserved Connection	

Click for FOQs on IQD Advance Clock Modules

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